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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/564,922	01/17/2006	Hendrik Ten Pierick	NL.0308834	5288

24737 7590 11/24/2008
PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
HASSAN, SARAH	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
11/24/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/564,922	TEN PIERICK ET AL.	
	Examiner	Art Unit	
	SARAH HASSAN	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 January 2006* is/are: a)☒ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14 are pending.

Priority

2. Foreign priority is acknowledged based on foreign application EP 03102241.1 filed on July 21, 2003.

Drawings

3. **The drawings are objected to because Figures 2-6 depict blocks with reference characters, but no labels or wording to properly identify the blocks**. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the

applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: **Reference 24 in Figures 2-4 are not described in the specification**. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 1-11, 12, 13, 14 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

7. As to claims 1-11, 12, 13, according to paragraph 0033 in the specification of the instant US application 10/564922, it states "the embodiments described can be realized in hardware or in software." Since independent apparatus claims 1, 12, 13 are reasonably read on the corresponding software portion of the disclosure, the claims will be treated as a whole as directed to entirely a software embodiment, not a hardware embodiment. Thus a 101 rejection is made.

8. Claim 14 is rejected under 35 U.S.C. 101 as not falling within one of the four statutory categories of invention. While the claims recite a series of steps or acts to be performed, a statutory "process" under 35 U.S.C. 101 must (1) be tied to another statutory category (such as a particular apparatus), or (2) transform underlying subject matter (such as an article or material) to a different state or thing (Reference the May 15, 2008 memorandum issued by Deputy Commissioner for Patent Examining Policy, John J. Love, titled "Clarification of 'Processes' under 35 U.S.C. 101"). The instant claims neither transform underlying subject matter nor positively tie to another statutory category that accomplishes the claimed method steps, and therefore do not qualify as a statutory process.

9. Also with regard to claim 14, a **"computer programming product"** not claimed as "**embodied in and executed by a computer-readable medium**" is descriptive material per se and is not statutory because it is not capable of causing functional change in the computer. Such claimed data structures do not define any structural and

functional interrelationships with the other claimed aspects of the invention, which permit the data structure's functionality to be realized. In contrast, a claimed "**computer readable medium encoded with a computer program when executed comprising**" defines structural and functional interrelationships between the data structure and the computer software and hardware components which permit the functionality to be realized, and is thus statutory.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. **Claims 1-2, 13, 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer et. al., US Patent No. 6140852 published on October 31, 2000 in view of Sawada, US Patent No. 5870591 published on February 9, 1999.**

12. As to claims 1, 12, and 13, Fischer teaches "a digitally controlled oscillator" [see Figure 2, item 204] "for generating a digital reference signal." The output of the "digitally controlled oscillator" is inputted into a divider circuit (106). The output of the divider circuit corresponds to "digital reference signal."

"a digital phase detector" [see Figure 2, item 202] "for determining a phase difference." Fishcer discloses a phase detector (202) that detects a phase difference between two inputted signals.

"first digital signal" [see Figure 2, item 'fout'] "is recovered by adding the determined phase difference" [see Figure 2, item 'MC'] "to the phase of the digital reference signal." Fischer discloses "first digital signal is recovered" where the "first digital signal" is the output of the digital controlled oscillator (204). This recovered digital signal is generated and changed variably because the digital phase detector (202) outputs a magnitude control signal ('MC') that adjusts and sets adjustment step size of the phase as detailed in col. 3, lines 51-62.

It should be noted however that Fischer does not specifically teach "a digital filter for filtering the digital input signal."

"filtered digital input signal."

On the other hand, Sawada teaches "a digital filter" [see Figure 32, item 536] "for filtering the digital input signal" [see Figure 32, item 535]. Sawada specifically teaches filtering the output signal of the ADC (535) or the "digital input signal."

"filtered digital input signal" [see Figure 32, item 535]. Sawada specifically teaches filtering the output signal of the ADC (535) or the "digital input signal."

It would have been obvious to one of ordinary skill in the art to combine the teachings of Fischer with the teachings of Sawada because Sawada provides a signal processor as detailed in Figure 32 that prevents circuit area from increasing and ensures a fast and efficient operating speed as detailed in col. 4, lines 25-27.

13. As to claim 2, Fischer teaches "an offset value is added to the phase" [see Figure 2, item 'Up', 'Down'] "of the recovered first digital signal" [see Figure 2, item 204]. Fischer discloses up and down signals that are generated by the phase detector (202) which corresponds to an "offset value." In addition phase detector (202) generates "MC" or magnitude control signal. Thus all three signals influence the output of the controlled oscillator (204) or "recovered first digital signal."

Sawada teaches "digital filter" [see Figure 32, item 535].

14. As to claim 14, Fischer teaches "generating a digital reference signal." The output of the "digitally controlled oscillator" is inputted into a divider circuit (106). The output of the divider circuit corresponds to "digital reference signal."

"determining a phase difference." Fishcer discloses a phase detector (202) that detects a phase difference between two inputted signals. One of the signal is the internally generated reference signal which is the output of the divider (106) and the other signal is an external digital signal.

"digitally add the determined phase difference" [see Figure 2, item 'MC'] "to the phase of the digital reference signal to recover the first signal" Fishcer discloses "first signal" where the "first signal" is the output of the digital controlled oscillator (204). This recovered digital signal is generated and changed variably because the digital phase detector (202) outputs a magnitude control signal ('MC') that adjusts and sets adjustment step size of the phase as detailed in col. 3, lines 51-62.

It should be noted however that Fischer does not specifically teach "filtering the digital input signal with a digital filter"

"digital input signal."

On the other hand, Sawada teaches "filtering the digital input signal with a digital filter" [see Figure 32, item 535]. Sawada specifically teaches filtering the output signal of the ADC (535) or the "digital input signal."

"digital input signal" [see Figure 32, item 535]. Sawada specifically teaches filtering the output signal of the ADC (535) or the "digital input signal."

It would have been obvious to one of ordinary skill in the art to combine the teachings of Fischer with the teachings of Sawada because Sawada provides a signal processor as detailed in Figure 32 that prevents circuit area from increasing and ensures a fast and efficient operating speed as detailed in col. 4, lines 25-27.

15. **Claim 3-11 rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer et. al., US Patent No. 6140852 published on October 31, 2000 in view of Sawada, US Patent No. 5870591 published on February 9, 1999, and further in view of Horner et. al., US Patent No. 5357544 published on October 18, 1994.**

16. As to claim 3, Fischer teaches "digital input signal" [see Figure 2, item 202]. Fischer discloses digital phase detector (202) that provides phase difference for two digital signals. One of the signals is an internally generated signal (fvar) and the other signal is an external signal which corresponds to "digital input signal."

It should be noted however that both Fischer, Sawada do not teach "a first digital mixer for frequency down-conversion of the digital input signal before filtering."

On the other hand, Horner teaches "a first digital mixer" [see Figure 2, item 26] "for frequency down-conversion" [see Figure 2, item 16] "of the digital input signal before filtering" [see Figure 2, item 18]. Horner teaches down converted digital signal outputted from the ADC that is provided to a digital mixer (26).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Fischer with the teachings of Sawada because Sawada provides a signal processor as detailed in Figure 32 that prevents circuit area from increasing and ensures a fast and efficient operating speed as detailed in col. 4, lines 25-27.

It would have been obvious to one of ordinary skill in the art to combine the teachings of Fischer, Sawada with the teachings of Horner because Horner overcomes technical circuit issues such as problems relating to jitter as a result of temperature for example. In addition, Horner overcomes cost issues relating to the digital composite signal decoding means as detailed in col. 3, lines 1-10.

17. As to claim 4, Horner teaches "the first digital mixer uses the digital reference signal as a mixing signal" [see Figure 2, item 24, 26]. Horner mixes the downconverted digital signal with a reference signal generated by the reference signal generator (24) at the mixer (26).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Fischer, Sawada with the teachings of Horner because Horner overcomes

technical circuit issues such as problems relating to jitter as a result of temperature for example. In addition, Horner overcomes cost issues relating to the digital composite signal decoding means as detailed in col. 3, lines 1-10.

18. As to claim 5, Fischer teaches "digital input signal" [see Figure 2, item 202]. Fischer discloses digital phase detector (202) that provides phase difference for two digital signals. One of the signals is an internally generated signal (fvar) and the other signal is an external signal which corresponds to "digital input signal."

"recovered first digital signal" [see Figure 2, item 204]. The output of digital oscillator (204) is the "recovered first digital signal" ('fout').

Horner teaches "is a stereo multiplex signal" [see Figure 2; col. 3, lines 19-20]. Horner teaches stereophonic receiver shown in Figure 2 that receives an analog signal that is typified in Figure 1, and then undergoes digital transformation with the help of ADC (18).

"a pilot signal" [see Figure 2, item 20]. Horner teaches signal processor (20) that provides locking to the pilot of the stereo composite signal as detailed in col. 2, lines 43-49.

19. As to claim 6, Horner teaches "a phase of a pilot signal" [see Figure 2, tem 36] "is multiplied with a multiplication factor" [see Figure 2, item 38] "to recover a second digital signal" [see Figure 2, item 40]. Horner discloses a stereo composite signal that includes an inherent phase by nature, that is inputted into the interpolator (36). The interpolator

also receives the phase difference between the composite signal and reference signal generator and also receives an outputted coefficient value (38). At the interpolator, provides a sum of partial products or "multiplication factors" of data points and the coefficients as detailed in col. 7, lines 2-6. The second data signal is then as a result recovered after recovering or extracting pilot signal from the composite stereo signal as detailed in col. 8, lines 13-19.

It would have been obvious to one of ordinary skill in the art to combine the teachings of Fischer, Sawada with the teachings of Horner because Horner overcomes technical circuit issues such as problems relating to jitter as a result of temperature for example. In addition, Horner overcomes cost issues relating to the digital composite signal decoding means as detailed in col. 3, lines 1-10.

20. As to claim 7, Horner teaches "the second digital signal is a suppressed carrier signal of the stereo multiplex signal" The second data signal is then as a result recovered after recovering or extracting pilot signal from the composite stereo signal as detailed in col. 8, lines 13-19, to provide left and right channel signals.

It would have been obvious to one of ordinary skill in the art to combine the teachings of Fischer, Sawada with the teachings of Horner because Horner overcomes technical circuit issues such as problems relating to jitter as a result of temperature for example. In addition, Horner overcomes cost issues relating to the digital composite signal decoding means as detailed in col. 3, lines 1-10.

21. As to claim 8, Horner teaches "a stereo decoder" [see Figure 2] "for decoding the stereo multiplex signal into at least a first and a second signal" [see Figure 2, item 40]. The second data signal is then as a result recovered after recovering or extracting pilot signal from the composite stereo signal as detailed in col. 8, lines 13-19, to provide left and right channel signals.

It would have been obvious to one of ordinary skill in the art to combine the teachings of Fischer, Sawada with the teachings of Horner because Horner overcomes technical circuit issues such as problems relating to jitter as a result of temperature for example. In addition, Horner overcomes cost issues relating to the digital composite signal decoding means as detailed in col. 3, lines 1-10.

22. As to claim 9, Horner teaches "the stereo multiplex signal comprises a sum signal and a difference signal" [see Figure 1]. Horner teaches stereo composite signal that includes sum signal and difference signal as detailed in Figure 1.

"a frequency down-converted difference signal" [see Figure 2, item 16].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Fischer, Sawada with the teachings of Horner because Horner overcomes technical circuit issues such as problems relating to jitter as a result of temperature for example. In addition, Horner overcomes cost issues relating to the digital composite signal decoding means as detailed in col. 3, lines 1-10.

23. As to claim 10, Horner teaches "the difference signal is frequency down-converted" [see Figure 2, item 16] "by means of the recovered suppressed carrier signal" [see Figure 2, item 40]. The difference signal typified in Figure 1 is downconverted with the help of downconverter (16) and digital processor (20) that includes recovering suppressed carrier or pilot signal with the help of pilot cancel block (40).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Fischer, Sawada with the teachings of Horner because Horner overcomes technical circuit issues such as problems relating to jitter as a result of temperature for example. In addition, Horner overcomes cost issues relating to the digital composite signal decoding means as detailed in col. 3, lines 1-10.

24. As to claim 11, Fischer teaches "the phase offset value" [see Figure 2, item 'Up', 'Down'] "of the recovered first digital signal" [see Figure 2, item 204]. Fischer discloses up and down signals that are generated by the phase detector (202) which corresponds to an "offset value." In addition phase detector (202) generates "MC" or magnitude control signal. Thus all three signals influence the output of the controlled oscillator (204) or "recovered first digital signal."

Horner teaches "difference signal" [see Figure 1].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SARAH HASSAN whose telephone number is (571)270-3456. The examiner can normally be reached on Monday through Friday (available 8:00 AM - 5:00PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571)272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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